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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/813,087	03/19/2001	Frank R. Bryant	10004055-1	1395

7590 08/27/2002

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EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/813,087	BRYANT ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the election filed July 18, 2002.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: a) 15 (See Page 5 Line 17). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: a) 34 (See Figure 1); 26 (See Figure 1); c) 92 (See Figure 1); d) 90 (See Figure 1); e) 132 (See Figure 2); f) 317 (See Figure 7); and g) 258 (See Figure 258). A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because of the following: a) reference character "127" has been used to designate both bulk and substrate body (See Page 8 Line 4 and Page 9 Line 18); b) reference character "13" has been used to designate both address and diode (See Figure 6 and Page 9 Line 18); and c) reference character "46" has been used to designate both primitive driveline and primitive signal interface (See

Page 8 Line 26 and Page 9 Line 23). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 8-10 and 18-20 are objected to because of the following informalities: a) the way the preamble is written it is not clear as to whether the claim is independent or dependent (ex: A printhead, comprising: the integrated circuit of claim 1;). For example, the way the preamble is written for dependent claims 2-7 is clear. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 5, 9, 10 and 18-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "bulk" (See Claim 5); and b) fluidically" (See Claims 9, 18 and 19). Claims 10 and 20 depend directly or indirectly from a rejected claim and are, therefore, also rejected under 35 U.S.C. 112, second paragraph for the reasons set above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 2, 6-9, 11, 12, 16-19, 21-24, 27 and 28 are rejected under 35 U.S.C. 103(a) as obvious over Hess et al. (U.S. Patent No. 5,122,812).

In regards to claim 1, Hess et al. ("Hess") discloses the following:

a) a substrate (70) (See Figure 11);

b) a transistor (74) formed in the substrate (See Figure 11);

c) an ejection element (109) coupled to the transistor wherein the ejection element is disposed over the substrate without an intervening field oxide layer (See Figure 11).

In regards to claim 1, Hess fails to disclose the following:

a) gate of the transistor forms at least one closed loop.

Although, Hess does not specifically disclose that the gate (78) forms a closed loop. It is well known that gates form loops.

In regards to claims 2 and 12, Hess discloses the following:

a) a dielectric layer disposed between the ejection element and the substrate having a thickness greater than 2,000 Angstroms (See Column 5 Lines 22-24).

In regards to claims 6 and 16, Hess fails to disclose the following:

a) the transistor is formed with without an active mask definition.

However, the limitation of "active mask definition" makes it a product by process claim. The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claims 7 and 17, Hess discloses the following:

a) transistor has a gate oxide formed with a layer of silicon dioxide (72) and a layer of silicon nitride (122) (See Figure 11).

In regards to claims 8 and 18, Hess discloses the following:

a) an orifice layer (140) defining a nozzle fluidically coupled to the ejection element and wherein the nozzle is further fluidically coupled to a fluid channel to deliver fluid to the ejection element (See Column 8 Lines 26-44).

In regards to claims 9 and 19, Hess discloses the following:

a) a body having a fluid reservoir fluidically coupled to the fluid channel of the printhead (See Figure 10); and

b) a pressure regulator for maintaining a negative pressure relative to the ambient air pressure to prevent the fluid within the printhead from drooling out of the nozzle without activation of the ejection element (See Column 8 Lines 39-41).

In regards to claim 11, Hess discloses the following:

a) a substrate (See Figure 11);

b) a set of transistors formed in the substrate (See Column 5 Lines 32 and 33 and Figure 11);

c) an ejection element coupled to the transistor wherein the ejection element is disposed over the substrate without an intervening field oxide layer (See Figure 11).

In regards to claim 11, Hess fails to disclose the following:

a) the transistors are formed with at least one closed loop.

Although, Hess does not specifically disclose that the gate forms a closed loop. It is well known that gates form loops.

In regards to claim 21, Hess discloses the following:

a) a substrate (See Figure 11);

b) a transistor positioned on the substrate, the transistor comprising a source region (76), a drain region (79), and a gate (78)positioned between the source region and the drain region (See Figure 11);

c) a layer of silicon dioxide disposed over the substrate, and
a layer of polycrystalline silicon (80) directly on the layer of silicon dioxide (See Figure 11);

d) a layer of dielectric material covering the substrate having a plurality of openings there through, the openings providing access the source region, the drain region, and the gate of the transistor (See Column 5 Lines 22-24);

e) a layer of electrically resistive material positioned on the layer of dielectric material and in direct electrical contact with the source region, the drain region, and the gate through the openings (See Column 6 Lines 5 and 6);

f) a layer of conductive material (100) affixed to a portion of the layer of electrically resistive material in order to form a multi-layer structure, the layer of electrically resistive material having at least one uncovered section capable of functioning as an ejection element, the layer of electrically resistive material being covered with the layer of conductive material at the source region, the drain region and the gate of the transistor (See Figure 11);

g) a portion of protective material positioned on the ejection element (See Figure 11); and

h) an orifice layer having at least one nozzle, the orifice layer secured to the portion of protective material having a section thereof removed directly beneath the nozzle in order to form a fluid well in order to impart energy from the ejection element (See Figure 11).

In regards to claim 21, Hess fails to disclose the following:

a) the gate forming a closed loop.

Although, Hess does not specifically disclose that the gate forms a closed loop. It is well known that gates form loops.

In regards to claim 22, Hess discloses the following:

a) the layer of electrically resistive material is comprised of a mixture of tantalum and aluminum (See Column 6 Lines 5 and 6).

In regards to claim 23, Hess discloses the following:

a) the layer of electrically resistive material is comprised of polycrystalline silicon (See Column 6 Lines 17 and 18).

In regards to claim 24, Hess discloses the following:

a) the layer of conductive material comprises a metal selected from the group consisting of aluminum, copper, and gold (See Column 6 Lines 50-52).

In regards to claim 27, Hess discloses the following:

a) the transistor has a gate oxide a layer of silicon nitride disposed between the gate and substrate (See Figure 11).

In regards to claim 28, Hess discloses the following:

a) a first passivation layer positioned on the ejection element, the first passivation layer being comprised of silicon nitride (See Column 7 Lines 33 and 34 and Figure 11);

b) a second passivation layer positioned on the first passivation layer, the second passivation layer being comprised of silicon carbide(See Column 7 Lines 49 and 50 and Figure 11);

c) a cavitation layer positioned on the second passivation layer, the cavitation layer being comprised of a metal selected from the group consisting of tantalum, tungsten, and molybdenum (See Column 7 Lines 66 and 67); and

d) a fluid barrier layer (130) positioned on the cavitation layer, the fluid barrier layer being comprised of plastic, the orifice layer being secured to the fluid barrier layer (See Column 8 Lines 7 and 8).

10. Claims 3, 13 and 25 are rejected under 35 U.S.C. 103(a) as obvious over Hess et al. (U.S. Patent No. 5,122,812) in view of Hess (U.S. Patent No. 4,719,477).

In regards to claims 3, 13 and 25, Hess fails to disclose the following:

a) dielectric layer is phosphosilicate glass.

However, Hess discloses a semiconductor device with a dielectric layer of phosphosilicate glass (See Page 3 Lines 56-59). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hess to include a dielectric layer of phosphosilicate glass as disclosed in Hess to aid in inhibiting the formation of phosphoric acid.

11. Claims 4, 14 and 26 are rejected under 35 U.S.C. 103(a) as obvious over Hess et al. (U.S. Patent No. 5,122,812) in view of Hawkins (U.S. Patent No. 4,951,063).

In regards to claims 4 and 14, Hess fails to disclose the following:

a) the dielectric layer is comprised of a layer of thermal oxide and a layer of phosphosilicate glass.

However, Hawkins et al. ("Hawkins") discloses a dielectric layer with a layer of thermal oxide and a layer of phosphosilicate glass (See Column 4 Lines 52-55). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hess to include a dielectric layer with a layer of thermal oxide and a layer of phosphosilicate glass as disclosed in Hawkins to aid in protecting and insulating the heating elements.

In regards to claim 26, Hess fails to disclose the following:

a) the dielectric layer comprises of a layer of thermal oxide.

However, Hawkins discloses a dielectric layer with a layer of thermal oxide (See Column 4 Lines 52-55). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hess to include a dielectric layer with a layer of thermal oxide as disclosed in Hawkins to aid in protecting and insulating the heating elements.

12. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as obvious over Hess et al. (U.S. Patent No. 5,122,812) in view of Burke et al. (U.S. Patent No. 5,639,386).

In regards to claims 10 and 20, Hess fails to disclose the following:

a) transport mechanism for moving the fluid cartridge in at least one direction with respect to a recording media.

However, Burke et al. ("Burke") discloses a transport mechanism (See Figure 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hess to include a transport mechanism as disclosed in Burke to aid in transporting the cartridge.

Conclusion

13. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Verret et al. (U.S. Patent No. 5,023,690) discloses a metal oxide semiconductor device; b) Wakabayashi et al. (U.S. Patent No. 5,055,859) discloses a thermal printhead; c) Fasen et al. (U.S. Patent No. 5,159,353) discloses a thermal inkjet printhead; d) Spangler et al. (U.S. Patent No. 5,343,064) discloses a single crystal SOI process; f) Ikeda et al. (U.S. Patent No. 5,455,612) discloses a liquid jet recording head; g) Schlais et al. (U.S. Patent No. 5,872,034) discloses an EPROM in high density CMOS; h) Chan et al. (U.S. Patent No. 6,034,410) discloses a MOSFET structure with planar surface; i) Silverbrook (U.S. Patent No. 6,273,544 B1) discloses an inkjet printhead having a self aligned nozzle; and j) Hopkins (U.S. Patent No. 2002/0033864 A1) discloses a thermal ink jet printhead system; k) Scardovi et al. (European Patent No. EP0752313A2) discloses an ink jet print head thermal working method; l) Scardovi et al. (European Patent No. EP0749834A2) discloses an ink jet print head with

integrated driving components; m) Hawkins et al. (European Patent No. 0494076A2) discloses an chip for a thermal ink jet printhead; n) Anagnostopoulos et al. (European Patent No. EP1219427A2) discloses heaters in the ink channels; o) Silverbrook (International Publication No. WO 00/23279) discloses improvements for ink jet printers.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

August 20, 2002

Stephen D. Meier
Primary Examiner